ABSTRACT OF THE DISCLOSURE

A clock signal recovery circuit that is implemented in a receiver of a universal serial bus (USB) and a method for recovering a clock signal. The clock signal recovery circuit comprises a phase detector, a bidirectional shift register, a multiphase clock signal generator, and a phase selector. The phase detector detects a difference in phases between received data and a predetermined recovery clock signal and generates a first control signal indicative of the detected phase difference. The shift register is shifted in response to the detected signal and outputs a second control signal. The multiphase clock signal generator receives a receiver clock signal having the same frequency as that of a clock signal used in a USB transmitter (from which the data is transmitted) and generates a plurality of phase clock signals, preferably, first through N-th phase clock signals having the same frequencies as that of the receiver clock signal and having differences of about (360/N)*I degree (°) (where N is an integer, and I is an integer equal to or greater than 0 and equal to or less than N-1) from a phase of the receiver clock signal, respectively. The phase selector selects one of the first through N-th phase clock signals in response to the second control signal and outputs the selected phase clock signal as the recovery clock signal. Preferably, N is an integer equal to or greater than 2 and equal to or less than 8.